PD-003-1203006 Seat No. _____

M. Sc. (Sem. III) (CBCS) Examination

June / July - 2018

ET - 4 : Physics

(Analog & Digital Systems)

Faculty Code : 003

Subject Code : 1203006

Time : $2\frac{1}{2}$ Hours] [Total Marks : **70**

Instructions : (1) All questions are compulsory.
(2) Number on right margin indicates marks.

1 Attempt any **seven** : **14**

(a) Draw schematic symbol for the 8-pin op-amp and label each pin.

(b) List the open-loop op-amp configurations. What do you mean by open-loop and closedloop op-amp configurations ?

(c) Define feedback. What are the different types of feedback used in Op-Amp ?

(d) Define filter. What are the different types of filters.

(e) List the ideal op-amp electrical characteristics.

(f) How many bits would you require if you want a resolution of at least 40 mV and the full scale range is 10 V ?

(g) Prepare truth table for the Boolean function : $F = A + B' \cdot C$.

(h) Write the BCD codes.

(i) Which of the following counters can be operated at higher clock frequency ? Ripple counter and synchronous counter

(j) Draw the circuit of 4-bit shift left register. How many clock pulses are required to store a 4-bit binary number serially ?

2 Answer the following : (any **two**)

(a) Discuss designing steps of differential amplifier from two identical emitter - biased circuits. **7**

(b) Define an operational amplifier. Draw block diagram of a typical op-amp and discuss function of each block. **7**

(c) Define following parameters : **7**

(i) CMRR

(ii) Slew rate

(iii) Power consumption

(iv) Output voltage swing.

3 (a) Derive necessary formulae for closed-loop voltage gain, input and output resistances with feedback in the case of voltage series feedback amplifier. **7**

(b) Draw and briefly discuss frequency responsive curves of active filters. **7**

OR

3 (a) A binary full adder circuit has three inputs : X_n, Y_n and previous carry C_{n-1} and two outputs SUM and CARRY. The canonical Boolean expressions for outputs are : **7**

$$S_n\left(C_{n-1}, X_n, Y_n\right) = \sum(1, 2, 4, 7)$$

$$C_n\left(C_{n-1}, X_n, Y_n\right) = \sum(3, 5, 6, 7)$$

Design binary full adder circuit using all 2-input NAND gates.

(b) Write a note on designing of BCD to Exces-3 code converter. **7**

4 Attempt any **two** :

(a) Draw the circuit of asynchronous Mode-8 counter and explain its operation with counting sequence and timing diagram. **7**

(b) Explain the logic and operation of 8-bit successive Approximation ADC with neat diagrams. **7**

(c) Write brief note on Ring counters. **7**

5 Attempt any **two** : **14**

(a) Voltage follower

(b) Zero-crossing detector

(c) 4-Bit magnitude comparator

(d) Tracking ADC.
